IN THE CLAIMS:

Claim 1. (**Currently Amended**) A method for prefetching a program stored in a ~~main~~ memory, the method comprising the steps of:

reading the program from the ~~main~~ memory, wherein the program includes a pseudo instruction and at least one branch instruction or at least one call instruction, the pseudo instruction being arranged before the ~~at least one~~ branch instruction or the call instruction and including an address for ~~the~~ a branch destination instruction ~~and an address for data~~ or a call destination instruction;

detecting the pseudo instruction with a first unit;

reading the instruction ~~and the data~~ from the ~~main~~ memory in accordance with the address for the branch destination instruction ~~and the address for the data~~ or the call destination instruction with the first unit when the pseudo instruction is detected;

storing the instruction ~~and the data~~ in a buffer; and

executing the stored instruction with a second unit.

Claim 2. (**Currently Amended**) The method of claim 1, wherein the first unit includes a pseudo instruction detection unit connected in parallel with the buffer, wherein the step of detecting the pseudo instruction includes supplying the program read from the ~~main~~ memory to the pseudo instruction detection unit in parallel with the buffer.

Claim 3. (**Currently Amended**) The method of claim 1, wherein the buffer includes first and second buffers connected in parallel to the ~~main~~ memory, and the

method further comprising a step of storing the instruction ~~and data~~ read from the ~~main~~ memory in the first buffer and storing the instruction ~~and the data~~ included in the detected pseudo instruction in the second buffer.

Claim 4. (**Currently Amended**) The method of claim 3, further comprising the steps of:

identifying that at least one instruction following the pseudo instruction has been transferred to the first buffer with the first unit when the pseudo instruction is detected; and

prefetching the instruction ~~and the data~~ from the ~~main~~ memory in accordance with the at least one instruction address ~~and the data address~~ with the first unit after the transfer of the at least one instruction to the first buffer has been identified.

Claim 5. (**Currently Amended**) The method of claim 4, further comprising the step of identifying that the corresponding instruction ~~and data are~~ is stored in the second buffer in accordance with the at least one instruction address ~~and the data address~~ when the pseudo instruction is detected, wherein the prefetch step is executed when the corresponding instruction ~~and data are~~ is not stored in the second buffer.

Claim 6. (**Currently Amended**) The method of claim 1, further comprising the steps of:

identifying that at least one instruction following the pseudo instruction has been transferred to the buffer with the first unit when the pseudo instruction is detected; and

prefetching the instruction and the data from the ~~main~~ memory in accordance with at least one instruction address ~~and data address~~ with the first unit after the transfer of at least one instruction to the buffer has been identified.

Claim 7. **(Currently Amended)** The method of claim 6, further comprising the step of identifying that the corresponding instruction ~~and data are~~ is stored in the buffer in accordance with the at least one instruction address ~~and data address~~ with the first unit when the pseudo instruction is detected, wherein the prefetch step is executed when the corresponding instruction ~~and data are~~ is not stored in the buffer.

Claim 8. **(Currently Amended)** A microcontroller, comprising:

a buffer, connected to a ~~main~~ memory, for storing a program read from the ~~main~~ memory, wherein the program includes a pseudo instruction and at least one branch instruction or at least one call instruction, the pseudo instruction being arranged before the ~~at least one~~ branch instruction or the call instruction and including an address for ~~the~~ a branch destination instruction ~~and an address for data~~ or a call destination instruction;

a first unit including,

a pseudo instruction detection unit, connected to the ~~main~~ memory, for detecting the pseudo instruction included in the program read from the ~~main~~ memory; and

an address control unit, connected to the ~~main~~ memory and the pseudo instruction detection unit, for reading the instruction ~~and data~~ from the ~~main~~ memory in accordance with the address for ~~the~~ a branch destination instruction ~~and the address for the data~~ or a call destination instruction when the pseudo instruction is detected and storing the instruction ~~and the data~~ in the buffer; and

a second unit connected to the buffer, for executing the instruction stored in the buffer.

Claim 9. (**Currently Amended**) The microcontroller of claim 8, wherein the buffer includes first and second buffers connected in parallel to the ~~main~~ memory, wherein the first buffer stores the instruction ~~and data~~ read from the ~~main~~ memory, and the second buffer stores the instruction ~~and data~~ included in the detected pseudo instruction.

Claim 10. (**Currently Amended**) The microcontroller of claim 9, wherein the address control unit identifies that the corresponding instruction ~~and data are~~ is stored in the second buffer in accordance with the at least one instruction address ~~and data address~~ when the pseudo instruction is detected and permits storage of the instruction ~~and the data~~ in the second buffer when the corresponding instruction ~~and data are~~ is not stored in the second buffer.

Claim 11. (**Currently Amended**) The microcontroller of claim 10, wherein the pseudo instruction detection unit is connected in parallel with the first buffer for the ~~main~~ memory.

Claim 12. (**Currently Amended**) The microcontroller of claim 8, wherein the address control unit identifies that the corresponding instruction ~~and data are~~ is stored in the buffer in accordance with the at least one instruction address ~~and data address~~ when the pseudo instruction is detected and permits storage of the instruction ~~and the data~~ in the buffer when the corresponding instruction ~~and data are~~ is not stored in the buffer.

Claim 13. (**Currently Amended**) The microcontroller of claim 12, wherein the pseudo instruction detection unit is connected in parallel with the buffer for the ~~main~~ memory.

Claim 14. (**Currently Amended**) A device for detecting a pseudo instruction present before a specific instruction, wherein the pseudo instruction is stored in a ~~main~~ memory and includes an opcode and an operand, and wherein the device is independent of an instruction execution unit for executing the specific instruction, the device comprising:

a detection circuit, connected to the ~~main~~ memory, for receiving the pseudo instruction read from the ~~main~~ memory and detecting the opcode included in the pseudo instruction; and

a detection timing circuit, connected to the detection circuit, for calculating instruction length or the number of operands of the pseudo instruction from the opcode when the pseudo instruction is detected and determining the transfer period of the opcode based on the instruction length or the number of operands, wherein the detection timing circuit supplies a signal for invalidating the opcode detection operation during an operand transfer period.

Claim 15. (**Cancelled**)

Claim 16. (**Currently Amended**) A microcontroller connected to a ~~main~~ memory which stores a program including instructions ~~and data~~, the microcontroller comprising:

an instruction execution unit for reading instructions ~~and data~~ from the ~~main~~ memory and processing the read instructions; and

a prefetch circuit unit that receives instructions ~~and data~~ read from the ~~main~~ memory in response to a fetch signal, and detects pseudo instructions included in the instructions ~~and data~~, wherein a pseudo instruction precedes a branch instruction or a call instruction and indicates the existence of the branch instruction or the call instruction, and wherein the prefetch circuit is independent of the instruction execution unit;

wherein the prefetch circuit unit includes,

a prefetch buffer connected between the instruction execution unit and the ~~main~~ memory for temporarily storing instructions ~~and data~~ being transferred from the ~~main~~ memory to the instruction execution unit,

a bus interconnecting the prefetch buffer and the ~~main~~ memory,

a pseudo instruction detection unit connected to the bus for detecting pseudo instructions among the instructions ~~and data~~ being transferred from the ~~main~~ memory to the prefetch buffer,

a holding circuit, connected to the bus and to the pseudo instruction detection unit, for storing operands of the pseudo instruction,

a pseudo instruction buffer for temporarily storing instructions ~~and data~~ fetched from a location in the ~~main~~ memory which is pointed to by the branch instruction or the call instruction following the pseudo instruction,

an address control unit for generating the fetch signal and for generating a ~~main~~ memory address which points to the address of a next word to be read from the ~~main~~ memory, and wherein when the pseudo instruction detection unit detects a pseudo instruction, the instructions ~~and data~~ pointed to by the pseudo instruction are fetched from the ~~main~~ memory by the address control unit and stored in the pseudo instruction buffer so that when the branch instruction or the call instruction following the pseudo instruction is processed by the instruction execution unit, if the branch or the call is taken, the instructions ~~and data~~ pointed to by the branch instruction have been prefetched and stored in the pseudo instruction buffer.

Claim 17. (**Currently Amended**) The microcontroller of claim 16, wherein the pseudo instruction detection unit further comprises:

a pseudo instruction detection circuit that receives at least a part of each of the instructions ~~and data~~ being transferred from the ~~main~~ memory to the prefetch buffer, detects an opcode of a pseudo instruction therefrom, and generates a detection signal; and

a shift register connected to the pseudo instruction detection circuit and receiving the detection signal, and generating a hold circuit enable signal, wherein when the hold circuit enable signal is active, the holding circuit stores the pseudo instruction operands being transferred on the bus.

Claim 18. (**Currently Amended**) The microcontroller of claim 17, wherein the holding circuit includes:

an additional information holding circuit that stores a first operand of the pseudo instruction;

an upper address holding circuit that stores a second operand of the pseudo instruction; and

a lower address holding circuit that stores a third operand of the pseudo instruction, wherein the second and third operands comprise a ~~main~~ memory address.

Claim 19. (**Cancelled**)

Claim 20. (**Cancelled**)

Claim 21. (**Cancelled**)

Claim 22. (**Cancelled**)

Claim 23. (**Cancelled**)

Claim 24. (**Cancelled**)

Claim 25. (**Previously Presented**) The method of claim 1, further comprising handling the pseudo instruction as a no-operation (NOP) instruction when the pseudo instruction is detected.

Claim 26. (**Currently Amended**) The method of claim 1, further comprising the second unit ignoring an address for the pseudo instruction when receiving the address for ~~the at least one~~ a branch destination instruction ~~and the address for data~~ or a call destination instruction to skip the pseudo instruction.

Claim 27. (**Cancelled**)

Claim 28. (**Previously Presented**) The microcontroller of claim 8, wherein the second unit handles the pseudo instruction as a no-operation (NOP) instruction when the pseudo instruction is detected.

Claim 29. (**Currently Amended**) The microcontroller of claim 8, wherein the second unit ignores an address for the pseudo instruction when receiving the address for

~~the at least one~~ a branch destination instruction ~~and the address for data~~ or a call destination instruction to skip the pseudo instruction.

Claim 30. (**Currently Amended**) A method for prefetching a program stored in a ~~main~~ memory, the method comprising the steps of:

reading the program from the ~~main~~ memory, wherein the program includes a pseudo instruction and at least one branch instruction or at least one call instruction, the pseudo instruction being arranged before the ~~at least one~~ branch instruction or the call instruction and including an address for ~~the~~ a branch destination instruction ~~and an address for data~~ or a call destination instruction;

detecting the pseudo instruction with a first unit;

prefetching the instruction ~~and data~~ in accordance with the detection of the pseudo instruction with the first unit when the pseudo instruction is detected; and

handling the pseudo instruction as a no-operation (NOP) instruction when the pseudo instruction is detected with a second unit.

Claim 31. (**Currently Amended**) A method for prefetching a program stored in a ~~main~~ memory, the method comprising the steps of:

reading the program from the ~~main~~ memory, wherein the program includes a pseudo instruction and at least one branch instruction or at least one call instruction, the pseudo instruction being arranged before the ~~at least one~~ branch instruction or the call

instruction and including an address for ~~the~~ a branch destination instruction ~~and an address for data~~ or a call destination instruction;

detecting the pseudo instruction with a first unit when the pseudo instruction is detected;

prefetching the instruction ~~and data~~ in accordance with the detection of the pseudo instruction with the first unit; and

when receiving the address for the ~~at least one~~ branch destination instruction ~~and the address for data~~ or the call destination instruction with a second unit, which is independent of the first unit, skipping the pseudo instruction and executing the prefetched instruction.

Claim 32. (**Currently Amended**) An apparatus for prefetching a program stored in a ~~main~~ memory, the apparatus comprising:

a first unit for reading the program from the ~~main~~ memory, wherein the program includes a pseudo instruction and at least one branch instruction or at least one call instruction, the pseudo instruction being arranged before the ~~at least one~~ branch instruction or the call instruction and including an address for ~~the~~ a branch destination instruction or ~~an address for data~~ a call destination instruction, and wherein the first unit detects the pseudo instruction and prefetches the instruction ~~and data~~ when the pseudo instruction is detected; and

a second unit for executing a no-operation (NOP) operation in accordance with the detection of the pseudo instruction.

Claim 33. (**Currently Amended**) An apparatus for prefetching a program stored in a ~~main~~ memory, the apparatus comprising:

a first unit for reading the program from the ~~main~~ memory, wherein the program includes a pseudo instruction and at least one branch instruction or at least one call instruction, the pseudo instruction being arranged before the ~~at least one~~ branch instruction or the call instruction and including an address for ~~the~~ a branch destination instruction or ~~an address for data~~ a call destination instruction, and wherein the first unit detects the pseudo instruction and prefetches the instruction ~~and data~~ when the pseudo instruction is detected; and

a second unit for executing the prefetched instruction, wherein the second unit ignores an address for the pseudo instruction when receiving the address for the ~~at least one~~ branch destination instruction or ~~the address for data~~ the call destination instruction to skip the pseudo instruction.

Claim 34. (**Currently Amended**) An apparatus for prefetching a program stored in a ~~main~~ memory, the apparatus comprising:

a first unit for reading the program from the ~~main~~ memory, wherein the program includes a pseudo instruction and at least one branch instruction or at least one call instruction, the pseudo instruction being arranged before the ~~at least one~~ branch instruction or the call instruction and including an address for ~~the~~ a branch destination instruction or ~~an address for data~~ a call destination instruction, and wherein the first unit reads the instruction ~~and data~~ from the ~~main~~ memory in accordance with the address for

the branch destination instruction ~~and the address for the data~~ or the call destination instruction when the pseudo instruction is detected, wherein the first unit includes a buffer for storing the instruction ~~and the data~~; and

a second unit for executing the stored instruction.

35. (New) The method of claim 1, wherein the stored instruction is executed in a next cycle after the branch instruction or the call instruction is executed.

36. (New) A method for prefetching a program stored in a memory, the method comprising the steps of:

reading the program from the memory, wherein the program includes a pseudo instruction and at least one data calling instruction, the pseudo instruction being arranged before the data calling instruction and including an address for calling data;

detecting the pseudo instruction with a first unit;

reading the data from the memory in accordance with the address for the calling data with the first unit when the pseudo instruction is detected;

storing the data in a buffer; and

executing the data calling instruction with a second unit.